4fsc Clock Generator
Monolithic IC MM1093

Outline

This IC generates a clock used for driving the CCD that configures a comb filter for Y/C separation, or for sampling A/D and D/A converters that configure a digital comb filter.
It has a built-in subcarrier oscillator (3.58MHz or 4.43MHz) synchronized to the input chroma signal, and a clock oscillator that is 4 times the latter. MM1093ND and NF are available for NTSC format, and MM1093PD and PF for PAL format.

Features

1. Built-in fsc synchronized to input chroma signal and 4fsc oscillators
2. Reduced number of external parts due to 1 pin VCXO
3. +5V single power supply

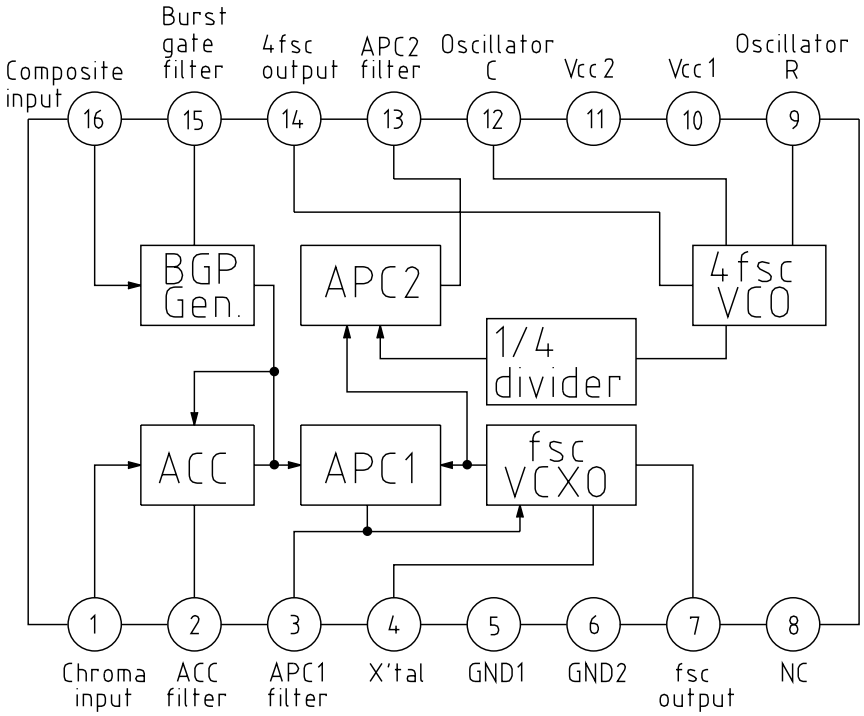
Package

SOP-16A (MM1093NF, MM1093PF)
DIP-16B (MM1093ND, MM1093PD)

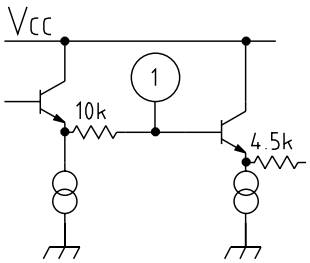
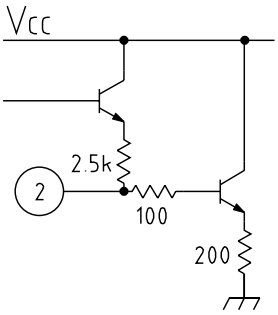
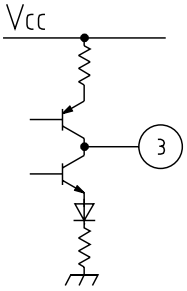
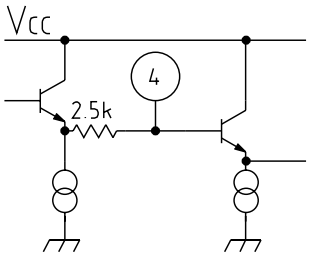
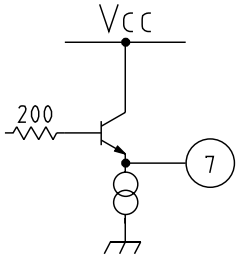
Applications

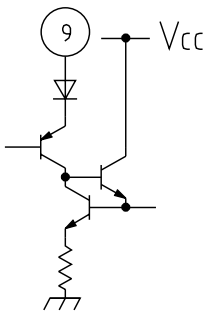
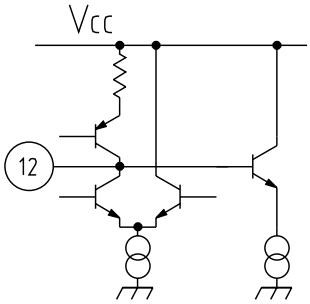
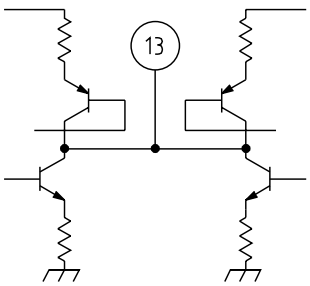
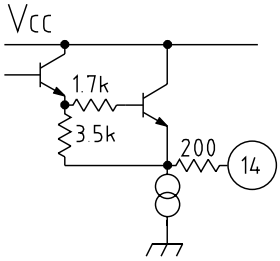
1. TV
2. VCR

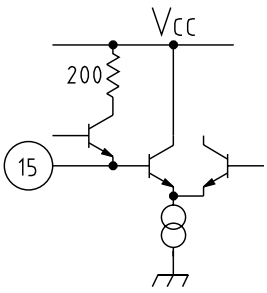
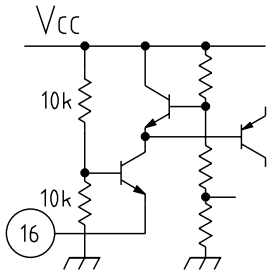
Equivalent Circuit Diagram



Pin Description

Pin no.	Pin name	Equivalent Circuit Diagram	Pin Description
1	Chroma input		Chroma signal input pin
2	ACC filter		ACC filter pin
3	APC1 filter		fsc APC circuit filter pin
4	X'tal		VCXO circuit X'tal pin
5	GND1		fsc GND pin
6	GND2		4fsc GND pin
7	fsc output		Outputs subcarrier synchronized to input chroma signal NTSC : 3.579545MHz PAL : 4.433619MHz

8	NC		NC pin
9	Oscillator R		Connects to resistor that determines 4fsc VCO free run frequency
10	Vcc1		fsc power supply pin
11	Vcc2		4fsc power supply in
12	Oscillator C		Connects to capacitor that determines 4fsc VCO free run frequency
13	APC2 filter		4fsc APC circuit filter pin
14	4fsc output		Outputs a 4× signal sychronized to input chroma signal.

15	Burst gate filter		This pin creates burst gate pulse.
16	Composite input		Composite signal input pin

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T_{STG}	–40~+125	°C
Operating temperature	T_{OPR}	–20~+75	°C
Power supply voltage	V_{CC} max.	7	V
Allowable loss	Pd	350	mW

Electrical Characteristics (Except where noted otherwise, Ta=25°C, V_{CC}=5.0V, SG1, SG2 : no signal, SW1 : A)

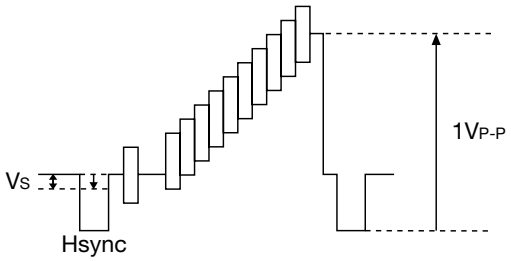
Item	Symbol	Measurement circuit	Measurement conditions	Min.	Typ.	Max.	Units
Operating power supply voltage	V_{CC}	V_{CC}		4.7	5.0	5.3	V
Consumption current	I_{CC}	–			24	32	mA
Sync separation circuit							
Sync separation level	V_S	TP3	SG2 : $1V_{P-P}$ staircase wave ∗1 SG1 : separate chroma signal SW1 : B ∗5	40	80	120	mV
PLL circuit							
ACC input amplitude range	V_{IN}	TP1	SG1 : separate chroma signal ∗2 ∗5	15		560	mV_{P-P}
APC1 frequency acquisition range	fc	TP2	SG1 : sine wave $143mV_{P-P}$ SG2 : $1V_{P-P}$ staircase wave ∗3	400			Hz
VCO1 free run frequency deviation	⊿f0		∗4	–250	0	250	Hz
fSC output level	Vo1		SG1 : separate chroma signal SG2 : $1V_{P-P}$ staircase wave ∗5	0.8	1.0	1.2	V_{P-P}
fSC output duty	Do1		SG1 : separate chroma signal SG2 : $1V_{P-P}$ staircase wave ∗5	45	50	55	%
4fSC circuit							
4fSC output level	Vo2	TP3	SG1 : separate chroma signal SG2 : $1V_{P-P}$ staircase wave SW1 : B ∗5	0.8	1.0	1.2	V_{P-P}
4fSC output DT	Do2		SG1 : separate chroma signal SG2 : $1V_{P-P}$ staircase wave SW1 : B ∗5	45	50	55	%
fSC leakage	Lfsc		SG1 : separate chroma signal SG2 : $1V_{P-P}$ staircase wave SW1 : B ∗5		50		dB

Notes:

∗1 Sync separation level

Measure the level where SG1 input signal and TP3 output signal synchronize when $1V_{P-P}$ staircase wave sync signal level is raised from 0V.

SG2 : $1V_{P-P}$ staircase wave



∗2 ACC input amplitude range

Defined as separate chroma signal burst signal amplitude that can be input to chroma input.

∗3 APC1 frequency pull-in range

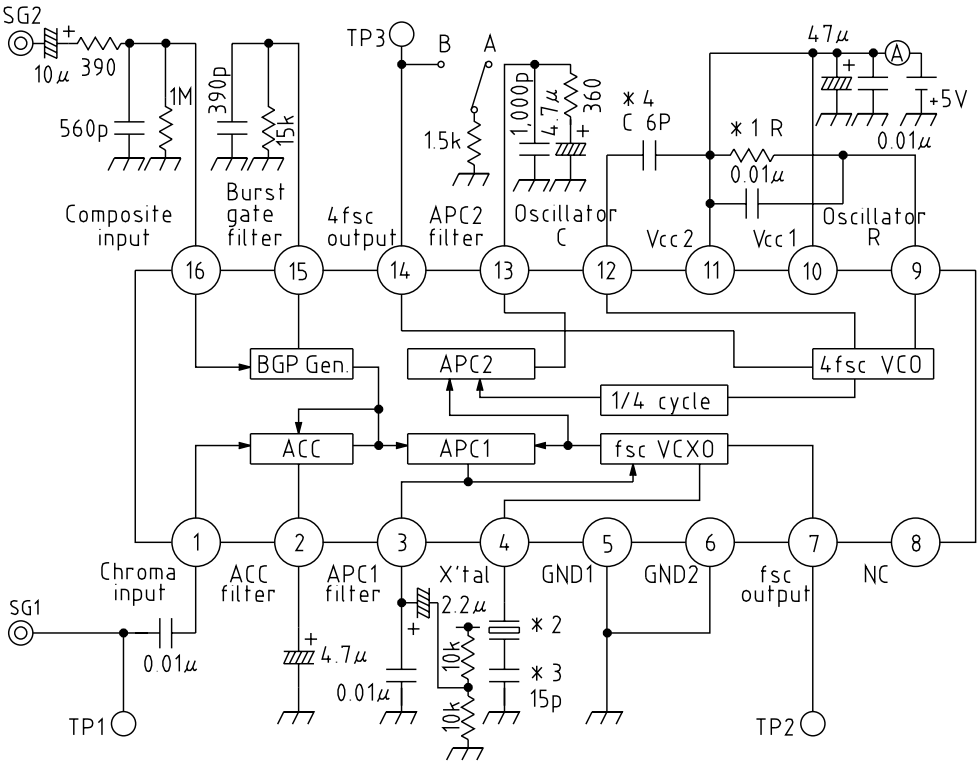
Defined as the smaller of the differences when input signal frequency is changed from high to f_O and from low to fo when TP2 output is not synchronized to SG1 input signal and when it is synchronized.

∗4 VCO1 free run frequency deviation

Defined as the difference between TP2 output signal frequency and f_O.

∗5 The standard for the separate chroma signal is burst signal $143mV_{P-P}$.

Measuring Circuit



Notes:

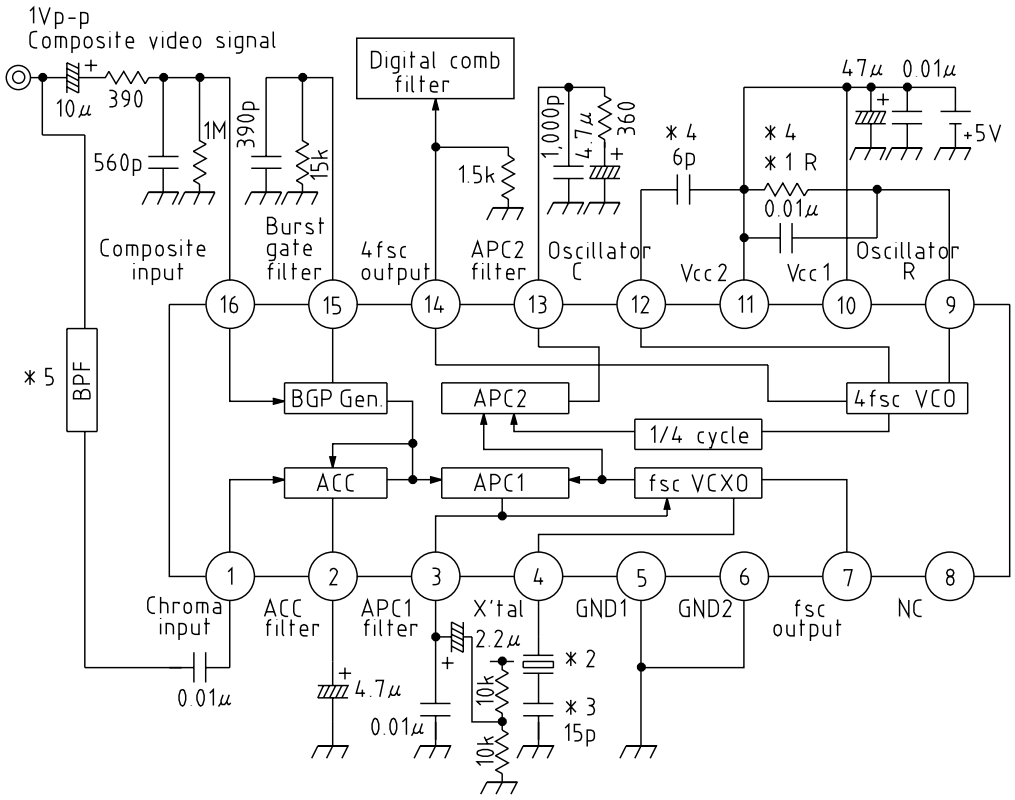
*1 NTSC : R=5.6k
PAL : 4.3k

*2 Recommended crystal oscillator
Tokyo Dempa, TR-49 or equivalent
NTSC : 3.579545MHz
PAL : 4.433619MHz

*3 Use part with precision within ±5% and temperature characteristic CH.

*4 R and C change according to board floating capacitance, etc. Select R and C so that Pin 13 voltage is approximately 2V for VCO lock. Also, C should be 4PF or higher, and R should be 3.3kΩ or higher.

Application Circuits



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*5 BPF Reference circuit